

Approved : Yoshimichi Hirokawa
Yoshimichi Hirokawa

Prepared : Yasuehiro Masuya
Yasuehiro Masuya

No.	Test item	Conditions	Conditions of acceptability	Result
1	High temp./overload test	(1) Input : Max.voltage, Min.voltage (2) Output : Overload (3) Test period : 48 hours (4) Testing circuit Fig.1~Fig.4	(1) Power supply is not failed.	OK
2	High voltage input test	(1) Input : 1.35 times of rated voltage (2) Output : Rated output (3) Ambient temp. : $25 \pm 10^\circ\text{C}$ (4) Testing circuit Fig.1~Fig.4	(1) No smoke, no fire.	OK
3	Low voltage input test	(1) Input : Min. regulation voltage (2) Output : Rated output (3) Ambient temp. : $25 \pm 10^\circ\text{C}$ (4) Test period : 48 hours (5) Testing circuit Fig.1~Fig.4	(1) Power supply is not failed.	OK
4	Input ON/OFF test	(1) Input : Max.voltage $T=2\text{sec}$ Duty= 50% (2) Output : Rated output (3) Ambient temp. : $25 \pm 10^\circ\text{C}$ (4) ON/OFF period : 1,000 (5) Testing circuit Fig.1~Fig.4	(1) Power supply is not failed. (2) The surge current of each components should not exceed the rated value.	OK
5	Output ON/OFF test	(1) Input : Rated input (2) Output : $0\% \leftrightarrow 100\%$ $T=2\text{sec}$ Duty= 50% (3) Ambient temp. : $25 \pm 10^\circ\text{C}$ (4) ON/OFF period : 1,000 (5) Testing circuit Fig.1~Fig.4	(1) Power supply is not failed.	OK
6	Output-short start test	(1) Input : Max.voltage (2) Output : Short start (3) Ambient temp. : $25 \pm 10^\circ\text{C}$ (4) Testing circuit Fig.1~Fig.4	(1) Power supply is not failed.	OK
7	Output short test	(1) Input : Max.voltage (2) Output : Short (3) Ambient temp. : $25 \pm 10^\circ\text{C}$ (4) Test period : 48 hours (5) Testing circuit Fig.1~Fig.4	(1) Power supply is not failed.	OK
8	Vibration/impact test	Vibration (1) $f=10 \sim 150\text{Hz}$: 49.0m/s^2 (2) 3 minutes period (3) 60 minutes along X, Y and Z axis Impact (1) 294.2m/s^2 11ms (2) Once each X, Y and Z axis	(1) No degradation of electric characteristics after test. (2) No crack at solder joint. (3) No marked damage of appearance.	OK

○ Testing circuitry

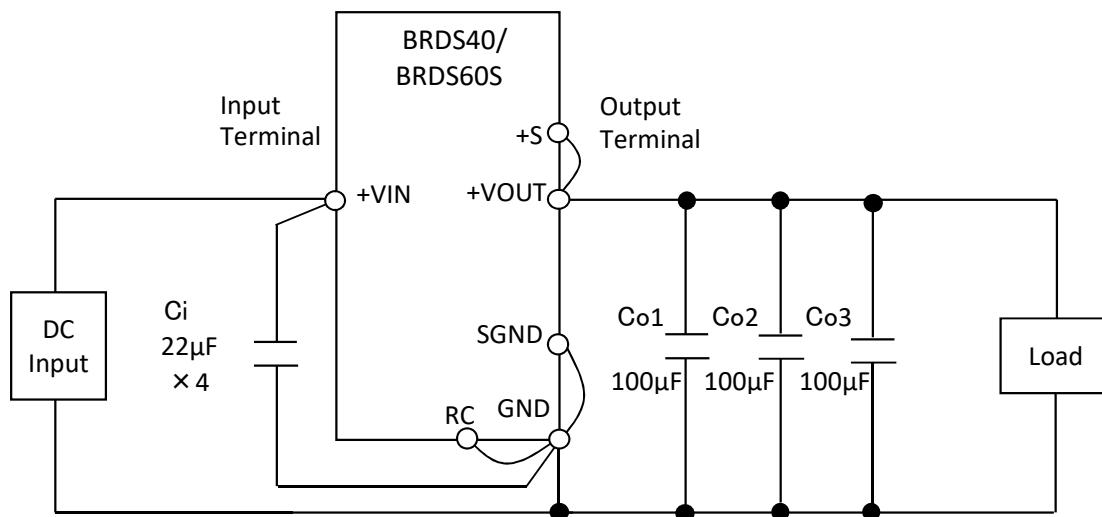


Fig.1 Testing circuitry (BRDS40/60S)

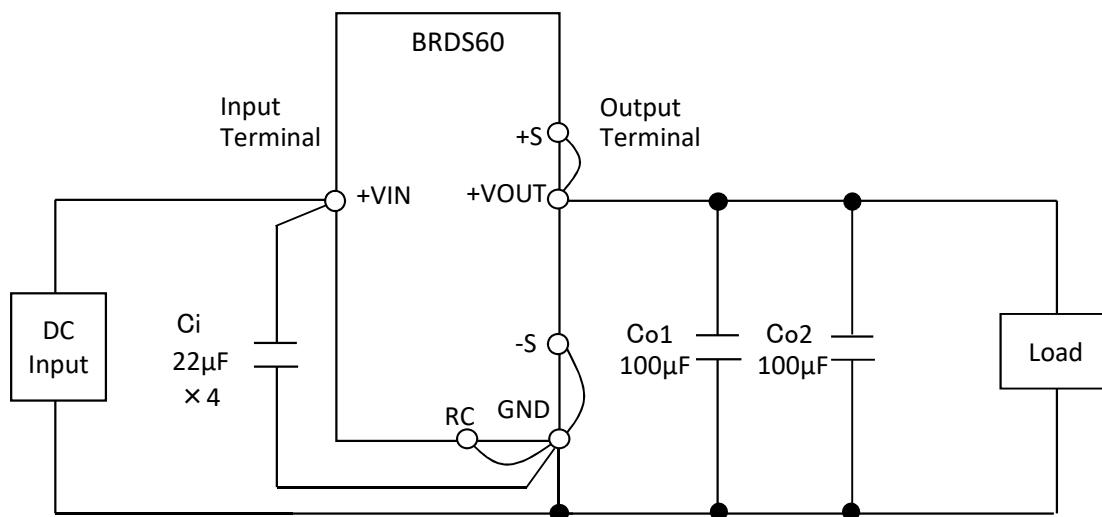


Fig.2 Testing circuitry (BRDS60)

○ Testing circuitry

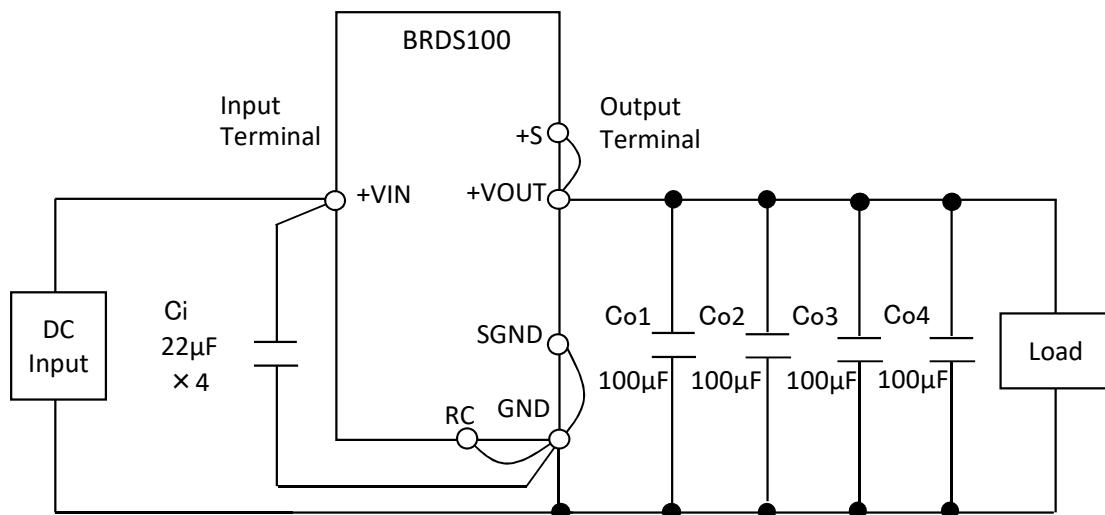


Fig.3 Testing circuitry (BRDS100)

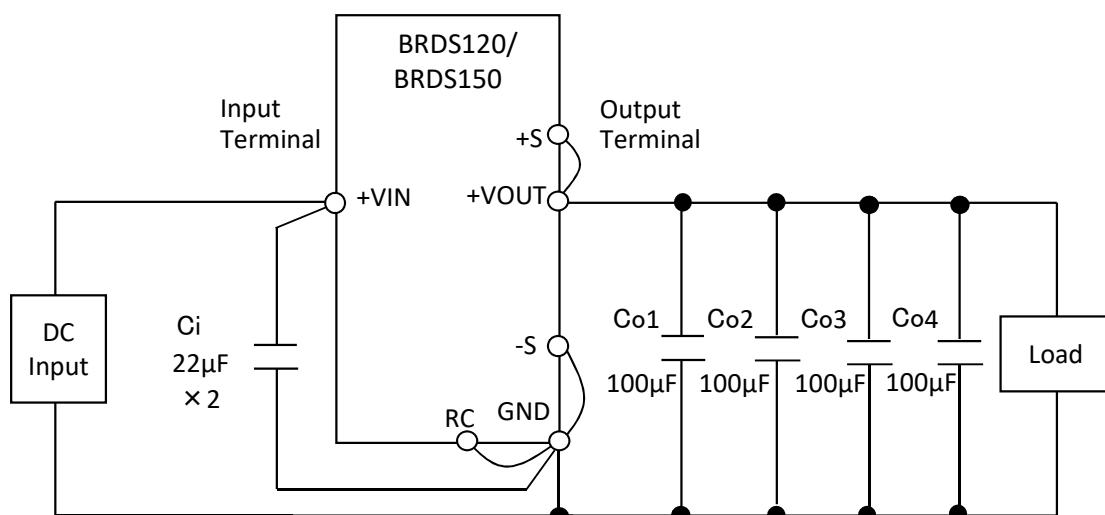


Fig.4 Testing circuitry (BRDS120/150)